PATENT NUMBER and ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10010162	11/20/2001	438	700	2812	ROMAN, A

**APPLICANTS: Hshieh Fwu-luan; So Koon; Amato John; Pratt Brian;

**CONTINUING DATA VERIFIED: none AR 06/30/03

** FOREIGN APPLICATIONS VERIFIED: none AR 06/30/03

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐	
Foreign priority claimed	☐ yes ☒ no		ATTORNEY DOCKET NO
35 USC 119 conditions met	☐ yes ☐ no		GS 149
Verified and Acknowledged Examiners's intials	AR 06/30/03		

TITLE : Method of forming narrow trenches in semiconductor substrates

U.S.DEPT OF COMM /PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED	Assistant Examiner	CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G
ISSUE FEE		DRAWING	
Amount Due / Date Paid	Primary Examiner	Sheets Drwg. / Figs.Drwg. / Print Fig.	
☐ TERMINAL DISCLAMER	PREPARED FOR ISSUE	Applicati n Examiner	

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